

CLAIMS:

1. A semiconductor processing method of forming a plurality
2 of conductive lines comprising the following steps:

3 providing a substrate;

4 providing a first conductive material layer over the substrate;

5 providing a first insulating material layer over the first conductive
6 layer;

7 etching through the first insulating layer and the first conductive
8 layer to the substrate to both form a plurality of first conductive lines
9 from the first conductive layer and provide a plurality of grooves
10 between the first lines, the first lines being capped by first insulating
11 layer material, the first lines having respective sidewalls;

12 electrically insulating the first line sidewalls; and

13 after insulating the sidewalls, providing the grooves with a second
14 conductive material to form a plurality of second lines within the
15 grooves which alternate with the first lines.

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18 2. The semiconductor processing method of forming a plurality
19 of conductive lines of claim 1 wherein the first lines have a
20 substantially common lateral cross sectional shape and the second lines
21 have a substantially common lateral cross sectional shape, the first lines'
22 lateral cross sectional shape being different from the second lines'
23 lateral cross sectional shape.

1 3. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 1 wherein the first and second conductive
3 materials are the same material.

4 5. The semiconductor processing method of forming a plurality
5 of conductive lines of claim 1 wherein the first and second conductive
6 materials are different materials.

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9 5. The semiconductor processing method of forming a plurality
10 of conductive lines of claim 1 wherein the first conductive material
11 comprises undoped polysilicon and the second conductive material
12 comprises metal.

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14 6. The semiconductor processing method of forming a plurality
15 of conductive lines of claim 1 wherein the first conductive material
16 comprises doped polysilicon and the second conductive material
17 comprises metal.

1 7. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 1 wherein the grooves have respective open
3 widths, and the step of electrically insulating the first line sidewalls
4 comprises:

5 depositing a second insulating material layer over the etched first
6 insulating and first conductive layers and the first line sidewalls to a
7 thickness which is less than one-half the respective groove open widths
8 to less than completely fill the grooves; and

9 anisotropically etching the second insulating material layer to
10 define insulating sidewall spacers over the first line sidewalls.

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12 8. The semiconductor processing method of forming a plurality
13 of conductive lines of claim 1 wherein the step of providing the grooves
14 with a second conductive material comprises:

15 depositing a second conductive material layer to a thickness
16 effective to fill the grooves; and

17 without photomasking, planarize etching the second conductive
18 material layer to form the plurality of second lines within the grooves.

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20 9. The semiconductor processing method of forming a plurality
21 of conductive lines of claim 1 further comprising forming a contact
22 opening into the substrate prior to providing the grooves with the
23 second conductive material.

1 10. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 1 further comprising forming a plurality of
3 series of the first and second conductive lines at multiple elevations
4 relative to the substrate.

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1 11. A semiconductor processing method of forming a plurality
2 of conductive lines comprising the following steps:
3 providing a substrate;
4 providing a first conductive material layer over the substrate;
5 providing a first insulating material layer over the first conductive
6 layer;
7 etching through the first insulating layer and the first conductive
8 layer to the substrate to both form a plurality of first conductive lines
9 from the first conductive layer and provide a plurality of grooves
10 between the first lines, the first lines being capped by first insulating
11 layer material, the first lines having respective sidewalls, the grooves
12 having respective open widths;
13 depositing a second insulating material layer over the etched first
14 insulating and first conductive layers and the first line sidewalls to a
15 thickness which is less than one-half the respective groove open widths
16 to less than completely fill the grooves;
17 anisotropically etching the second insulating material layer to
18 define insulating sidewall spacers over the first line sidewalls;
19 after providing the insulating sidewall spacers, depositing a second
20 conductive material layer to a thickness effective to fill the remaining
21 grooves; and
22 without photomasking, planarize etching the second conductive
23 material layer to form a plurality of second lines within the grooves
24 which alternate with the first lines.

1 12. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 11 wherein the first lines have a
3 substantially common lateral cross sectional shape and the second lines
4 have a substantially common lateral cross sectional shape, the first lines'
5 lateral cross sectional shape being different from the second lines'
6 lateral cross sectional shape.

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8 13. The semiconductor processing method of forming a plurality
9 of conductive lines of claim 11 wherein the first and second conductive
10 materials are the same material.

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12 14. The semiconductor processing method of forming a plurality
13 of conductive lines of claim 11 wherein the first and second conductive
14 materials are different materials.

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16 15. The semiconductor processing method of forming a plurality
17 of conductive lines of claim 11 wherein the first conductive material
18 comprises undoped polysilicon and the second conductive material
19 comprises metal.

1 16. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 11 wherein the first conductive material
3 comprises doped polysilicon and the second conductive material
4 comprises metal.

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6 17. The semiconductor processing method of forming a plurality
7 of conductive lines of claim 11 wherein the first and second insulating
8 materials predominately comprise SiO₂.

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10 18. The semiconductor processing method of forming a plurality
11 of conductive lines of claim 11 further comprising forming a contact
12 opening into the substrate prior to depositing the second conductive
13 material.

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15 19. The semiconductor processing method of forming a plurality
16 of conductive lines of claim 11 further comprising forming a plurality
17 of series of the first and second conductive lines at multiple elevations
18 relative to the substrate.

1 20. A semiconductor processing method of forming a plurality
2 of conductive lines comprising the following steps:

3 providing a substrate;
4 providing a first conductive material layer over the substrate;
5 etching through the first conductive layer to the substrate to both
6 form a plurality of first conductive lines from the first conductive layer
7 and provide a plurality of grooves between the first lines, the first lines
8 having respective sidewalls;
9 electrically insulating the first line sidewalls; and
10 after insulating the sidewalls, providing the grooves with a second
11 conductive material to form a plurality of second lines within the
12 grooves which alternate with the first lines.

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14 21. The semiconductor processing method of forming a plurality
15 of conductive lines of claim 20 wherein the first lines have a
16 substantially common lateral cross sectional shape and the second lines
17 have a substantially common lateral cross sectional shape, the first lines'
18 lateral cross sectional shape being different from the second lines'
19 lateral cross sectional shape.

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21 22. The semiconductor processing method of forming a plurality
22 of conductive lines of claim 20 wherein the first and second conductive
23 materials are the same material.

1 23. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 20 wherein the first and second conductive
3 materials are different materials.

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5 24. The semiconductor processing method of forming a plurality
6 of conductive lines of claim 20 wherein the grooves have respective
7 open widths, and the step of electrically insulating the first line
8 sidewalls comprises:

9 depositing a second insulating material layer over the etched first
10 conductive layers and the first line sidewalls to a thickness which is less
11 than one-half the respective groove open widths to less than completely
12 fill the grooves; and

13 anisotropically etching the second insulating material layer to
14 define insulating sidewall spacers over the first line sidewalls.

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16 25. The semiconductor processing method of forming a plurality
17 of conductive lines of claim 20 wherein the step of providing the
18 grooves with a second conductive material comprises:

19 depositing a second conductive material layer to a thickness
20 effective to fill the grooves; and

21 without photomasking, planarize etching the second conductive
22 material layer to form the plurality of second lines within the grooves.

1 26. The semiconductor processing method of forming a plurality
2 of conductive lines of claim 20 wherein the grooves have respective
3 open widths, and the step of electrically insulating the first line
4 sidewalls comprises:

5 depositing a second insulating material layer over the etched
6 first conductive layers and the first line sidewalls to a thickness
7 which is less than one-half the respective groove open widths to
8 less than completely fill the grooves; and

9 anisotropically etching the second insulating material layer
10 to define insulating sidewall spacers over the first line sidewalls;
11 and

12 the step of providing the grooves with a second conductive
13 material comprises:

14 depositing a second conductive material layer to a thickness
15 effective to fill the grooves; and

16 without photomasking, planarize etching the second
17 conductive material layer to form the plurality of second lines
18 within the grooves.

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1 27. Integrated circuitry comprising:

2 a substrate; and

3 a series of alternating first and second conductive lines provided
4 relative to the substrate, the first and second lines being spaced and
5 positioned laterally adjacent one another relative to the substrate, the
6 first lines and the second lines being electrically isolated from one
7 another laterally by intervening anisotropically etched insulating spacers
8 formed laterally about only one of the first or second series of lines.

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10 28. The integrated circuitry of claim 27 wherein the first lines
11 have a substantially common lateral cross sectional shape and the
12 second lines have a substantially common lateral cross sectional shape,
13 the first lines' lateral cross sectional shape being different from the
14 second lines' lateral cross sectional shape.

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16 29. The integrated circuitry of claim 27 wherein the first and
17 second conductive lines constitute the same materials.

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19 30. The integrated circuitry of claim 27 wherein the first and
20 second conductive lines constitute different materials.

1 31. The integrated circuitry of claim 27 wherein the first
2 conductive lines predominately comprise undoped polysilicon and the
3 second conductive lines predominately comprise metal.

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5 32. The integrated circuitry of claim 27 wherein the first
6 conductive lines predominately comprise doped polysilicon and the second
7 conductive lines predominately comprise metal.

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9 33. The integrated circuitry of claim 27 comprising a plurality
10 of the series of the first and second conductive lines at multiple
11 elevations relative to the substrate.

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13 34. Integrated circuitry comprising:
14 a substrate; and
15 a series of alternating first and second conductive lines provided
16 relative to the substrate, the first and second lines being spaced and
17 positioned laterally adjacent one another relative to the substrate, the
18 first lines and the second lines being electrically isolated from one
19 another laterally by intervening strips of insulating material, the first
20 lines having a substantially common lateral cross sectional shape and the
21 second lines having a substantially common lateral cross sectional shape,
22 the first lines' lateral cross sectional shape being different from the
23 second lines' lateral cross sectional shape.

1 35. The integrated circuitry of claim 34 wherein the first and
2 second conductive lines constitute the same materials.

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4 36. The integrated circuitry of claim 34 wherein the first and
5 second conductive lines constitute different materials.

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7 37. The integrated circuitry of claim 34 wherein the first
8 conductive lines predominately comprise undoped polysilicon and the
9 second conductive lines predominately comprise metal.

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11 38. The integrated circuitry of claim 34 wherein the first
12 conductive lines predominately comprise doped polysilicon and the second
13 conductive lines predominately comprise metal.

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15 39. The integrated circuitry of claim 34 comprising a plurality
16 of the series of the first and second conductive lines at multiple
17 elevations relative to the substrate.